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PATENT APPLICATION

LASER ALIGNMENT TARGET

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LASER ALIGNMENT TARGET

This application claims the benefit of U.S. Provisional Application Number 60/015,119, filed April 10, 1996, incorporated herein by reference.

BACKGROUND OF THE INVENTION

The present invention relates generally to the field of integrated circuit fabrication. More specifically, the present invention is structure and a technique for fabricating a structure useful for aligning a wafer, substrate, or integrated circuit die.

There are many circumstances where aligning a wafer or integrated circuit die is important. For example, alignment is important during the processing of integrated circuits. Integrated circuits are fabricated using a layer-by-layer process. Alignment may be critical during the processing of certain layers, where these layers must to aligned properly in relationship to previous layers. For example, a contact layer must be aligned properly with a first conductor layer in order to create contacts at the correct locations. Contacts formed at the wrong locations may create shorts or opens, and reduce yield.

Proper alignment is also critical in many other situations. These include testing of an integrated circuit die on a wafer. The die must be positioned properly in order to properly probe the device.

Moreover, alignment is also important when programming or configuring an integrated circuit. For example, a die may have fuses that are to be laser programmed. The fuses may be made of polysilicon, or another conductor. This fuse may couple together two (or more) devices or conductors. A laser with sufficient energy is directed at the fuse. The laser "blows" the fuse, decoupling the two devices or conductors. In order for the laser to properly reference

the coordinates of a fuse, the integrated circuit must be aligned properly. When the integrated circuit is not aligned properly, the laser may damage or destroy a portion of the circuitry instead of blowing the desired fuse. Therefore, the alignment of an integrated circuit or wafer is especially critical.

A wafer or integrated circuit die may need to be aligned properly in an X-direction, Y-direction, rotation angle, and other orientation. As technology improves, alignment is becoming more important and critical, especially resulting from the continued scaling and shrinking of semiconductor device geometries. Integrated circuits (or "chips") have progressively become smaller and denser, and any small misalignment will adversely affect the integrated circuit yield and functionality of the integrated circuit.

One technique of alignment is by use of an alignment target. An alignment target should have good reflective or optical contrast so it can be easily identifiable. For example, a laser may be used to determine a change in reflectivity or optical contrast in a semiconductor structure used as the alignment target. This contrast may be achieved by forming a region with rough topology and a region into a smooth topology, where these regions are in close proximity to one another. Light is reflected from the smooth or planar region while light is scattered from the rough region. A laser alignment system would find this alignment target and align the wafer or integrated circuit based on the target.

In order to facilitate the fabrication of smaller device sizes, current process technologies emphasize relatively smooth or planar topologies. Smooth topologies allow better step coverage and allow packing of devices and geometries closer together. Some of the techniques used to form flat topologies include such processing techniques as chemical-mechanical polishing (CMP). With CMP, process layers (e.g., dielectrics) are mechanically polished with a slurry mixture to form a very flat topology. A further technique includes plug technology (e.g., tungsten plug technology), where a plug material is used to fill contacts or vias, or

both, in order to minimize step coverage (i.e., metal step cover over plugs may be near 100 percent). Plug technology further emphasizes a flat or planar topology.

Despite the substantial success of such planarized process technologies, these processes also meet with certain limitations, especially when used to create a region having good reflectivity, which may be used as an alignment target. With flat or smooth topologies, the resulting structures and regions will have a similar optical reflectiveness. This leads to poor reflective or optical contrast, making it difficult (and possibly impossible) to align a wafer or integrated circuit die, especially by using laser. Furthermore, in some processes, metals use antireflective coatings, further reducing the reflectivity contrast over flat topology.

As can be seen, a structure and technique for fabricating a good reflective contrast is needed, especially where this structure is useful as an alignment target for aligning a wafer or integrated circuit.

SUMMARY OF THE INVENTION

The present invention is a structure and technique for fabricating a structure having good reflective contrast for use as an alignment structure. In particular, a technique of the present invention is for fabricating a structure having a rough topology using a planarized semiconductor process. The rough topology structure of present invention has a different reflectivity compared to a smooth or planar topology structure. Specifically, the rough topology will scatter incident radiation and light, while the smooth topology will reflect radiation and light. A structure including both rough and smooth topologies may be used as an alignment target for aligning an integrated circuit or wafer. The system will be able to identify the reflective and optical contrast between the smooth and rough topology. After alignment, an integrated circuit, such as a memory, microprocessor, or programmable logic device, may be programmed, such as by a laser to blow laser-programmable fuses.

The technique of the present invention includes forming an initial cored region in a plug filling a contact opening. This cored region is nonplanar and has a depression in about the middle of the contact opening. Subsequent
5 process layers are formed on top of this depression. The subsequent process layers also have a depression and are nonplanar above the cored region in the contact layer. The subsequent process layers generally aggravate or augment the nonplanar characteristics of the cored region. Also,
10 subsequent via layers may also be cored, similar to the contact layer, to further enhance the roughness of the topology.

More specifically, the method of forming a rough topology on a substrate using a planarized process of the
15 present invention includes the following steps. A contact opening is formed where a lateral dimension of the contact opening exceeds a minimum contact size. The contact opening is filled with a first plug layer. The first plug layer is etched back to create a first cored region in the first plug
20 layer. The first cored region has a first depression. A subsequent process layer is formed and stacked on the first cored region. The subsequent process layer has a second depression formed on top of the first depression. In a specific embodiment, at least one lateral dimension of the
25 contact opening exceeds about 1.5 times the minimum contact size.

Moreover, an alignment structure for semiconductor fabrication of the present invention includes a smooth and a rough region formed on a substrate. The rough region includes
30 a first conductive layer and a second conductive layer formed above the first conductive layer. A first insulating layer is formed between the first and second conductive layers. The first insulating layer has a first opening for electrically coupling the first and second conductive layers. A plug
35 layer, having a cored region, fills the first opening. The topological roughness formed by the cored region scatters incident radiation.

Other objects, features, and advantages of the present invention will become apparent upon consideration of the following detailed description and the accompanying drawings, in which like reference designations represent like features throughout the figures.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows alignment targets and an integrated circuit with programmable fuses;

Fig. 2A shows a top view of an alignment structure of the present invention;

Fig. 2B shows a top view of another embodiment of an alignment structure of the present invention;

Fig. 3 shows a cross-section of a planarized plug and contact opening;

Fig. 4 shows a cross-section of an alignment structure of the present invention;

Fig. 5 shows a cross-section of a contact opening;

Fig. 6 shows a cross-section of a plug layer filling a contact opening;

Fig. 7 shows a cross-section of coring in the plug of a contact opening; and

Fig. 8 shows a cross-section of coring in a conductor layer over the contact opening.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Fig. 1 is a diagram of an integrated circuit 110 and alignment targets 120. Integrated circuit 110 may be one of many on a wafer. Alignment targets 120 are used to align the integrated circuit. For example, alignment targets 120 may be used in the laser alignment of integrated circuit 110. Alignment targets 120 may also be used to align other objects and structures, such as entire wafers.

In the embodiment in Fig. 1, the alignment targets are shown as L-shaped structures. Many other shapes and sizes of alignment targets may be used including crosses ("X's"), pluses ("+'s"), and tees ("T's"), just to name a few. The

shape and size of the structure are selected to permit easy and precise alignment.

For more precise alignment, the alignment targets should be positioned relatively close to the structure to be aligned. Specifically, in Fig. 1, alignment targets 120 are placed adjacent to, but outside integrated circuit 110. Moreover, for example, alignment targets 120 may be in a die seal or scribe line adjacent particular dies within a wafer.

In further embodiments of the present invention, the alignment targets may also be placed within integrated circuit 110. In some circumstances, this may be necessary because of the processing requirements. Further, this may be necessary, for example, when aligning integrated circuit dies which have already been sawed from the wafer. However, having alignment targets within the integrated circuit may be somewhat undesirable because it reduces the amount of usable area within the integrated circuit.

Alignment targets may be used to align multiple or groupings of integrated circuit dies at the same time. For example, an array of two rows by three columns of integrated circuit dies may use the same set of alignment targets. Since more than one die may be "group aligned" simultaneously, this approach may save time when aligning the integrated circuits. Also, since fewer alignment targets are needed, less area is used by the alignment targets, so more dies may be placed on a wafer. This technique may be used in a multiple-die reticle field. As all the die in a reticle field are exposed at one time, there is no relative variation between the die. However, different reticle steppings may have movement variations; then, separate alignment is typically required.

For alignment, a pair of alignment targets may be used, such as shown in Fig. 1. However, there may be any number of alignment targets, sufficient to allow for precise and accurate alignment. The integrated circuit may need to be aligned in several different directions and angles, including, for example, an X-direction, Y-direction, and rotation angle. The number and shape of the alignment targets should be selected to allow the desired alignment approach.

A particular application, among many others, where alignment of integrated circuits is especially important is the laser programming of fuses within the dies. As shown in Fig. 1, there may be one of more fuses 130 within the integrated circuit. Each may control a particular feature. For example, fuse-programmable options may be used to repair against low-level defects in integrated circuits. If a defect is found in a particular circuit, then after the integrated circuit has been aligned using the alignment targets, a laser is referenced to a selected fuse location with the integrated circuit. The laser "blows" the fuse, which may be made of polysilicon or metal, in order to enable or disable the appropriate circuitry.

Alignment is especially critical since the laser must properly reference the precise location on the integrated circuit to program the fuse. For example, fuses may occupy less than 100 square micron area. Any misalignment error, and the laser may damage a portion of the integrated circuit.

Laser programming may also be employed in implementing redundancy of integrated circuit chips. With redundancy, some defective elements of a die can be replaced with nondefective extra resources provided for the repair. The accuracy of the replacement depends on the accuracy of laser programming.

Laser programming may be useful for configuring various types of integrated circuits including, but not limited to, memories, microprocessor, ASICs, gate arrays, field programmable gate arrays (FPGAs), and programmable logic devices (PLDs). For example, for PLDs, laser programming may be used to configure the logical elements and interconnections within between the logical elements. PLDs are typically programmed by electrically programming fuses, antifuses, EPROM, Flash, EEPROM, or SRAM cells.

Programmable logic integrated circuits and their operation are well known to those of skill in the art. See, for example, U.S. Patent Number 4,617,479, incorporated herein by reference for all purposes. Such devices are currently represented by, for example, Altera's MAX® series of PLDs and

FLEX[®] series of PLDs. The former are described in, for example, U.S. Patent Numbers 5,241,224 and 4,871,930, and the Altera Data Book, March 1995, all incorporated herein by reference. The latter are described in, for example, U.S. Patent Numbers 5,258,668, 5,260,610, 5,260,611 and 5,436,575, and also the Altera Data Book, March 1995, all incorporated herein by reference for all purposes.

Laser programming may be used in place of, or to supplement, the electrical configuration of PLDs. For example, laser programming may be used to program the programmable interconnect array (PIA), global interconnect, local interconnect, and other interconnection within a PLD. Laser programming may also be used to configure the functionality of logic array blocks (LABs) and logic elements (LEs). As a further example, a look-up table in a PLD may be configured by the way of laser programming.

The integrated circuit may be programmed in part by laser programming, then further electrically configured or programmed by a user. The user may program the device using a programmer device or using in-system programming (ISP). ISP involves electrically programming an integrated circuit while it resides on a system board. For example, a laser may program a portion of the global interconnect; and if desirable or necessary, the remaining portion of the global interconnect is configured in the field (i.e., by a customer or user).

Laser programming may be used to implement some features which are typically implemented using mask-programmable options. Mask-programmable options are features of the integrated circuit which are enabled or disabled by using an appropriate mask during a masking step. These options are usually implemented during a metal masking step, such as first or second metal layers. Although mask-programmable options are an effective technique, laser programming offers many advantages. For example, among other advantages, laser programming may lower overall production cost since integrated circuit dies do not need to be laser programmed until just before the parts are needed. Generic (unconfigured) parts may be stored in inventory and laser

configured as needed. This eliminates the need of keeping an inventory in various customized and specialized products.

Fig. 2A shows an embodiment of an alignment target 210 of the present invention. Here, alignment target 210 is an "L" shape; however, as discussed above, the alignment target may be many other shapes. Alignment target 210 may be mirrored, rotated, and positioned as desired on the wafer or integrated circuit.

Alignment target 210 includes a rough topology 220 and a smooth topology 230. Rough topology 220 and smooth topology 230 have a dissimilar optical reflectiveness. Generally, smooth topology 230 reflects incident radiation or light while rough topology 220 scatters incident radiation or light. Furthermore, on a wafer, especially one processed using a planarized process, areas (e.g., substrate, active regions) other than rough topology 220 will generally be highly reflective regions like smooth topology 230.

Fig. 2B illustrates an alternative embodiment of the alignment structure. In this embodiment compared to Fig. 2A, rough topology regions 220 are reversed with smooth topology regions 230. Use and fabrication of this alignment structure would be analogous to that for the structure shown in Fig. 2A.

An alignment system (which may use a laser) scans alignment target 210 and can recognize a difference in reflectivity between rough topology 220 and smooth topology 230. Using alignment target 210, the alignment system makes adjustments to position the wafer or integrated circuit into proper alignment. For example, a laser may scan alignment target 210 along a line and direction from 250 to 255. While scanning the alignment target, the scanning instruments will detect the difference in reflectivity between rough topology 220 and smooth topology 230. The reflectivity changes at an interface 270 between rough topology 220 and smooth topology 230.

In addition, there should be adequate space around the alignment mark so that circuitry or other features may not be mistaken for the alignment mark. Furthermore, the laser alignment may scan multiple times, such as in the X and Y

directions. And, there may be multiple scan marks. In a preferred embodiment, three alignment marks are used. A more precise alignment will result when using four or more targets.

Consequently, it is desirable that there is a high degree of reflective contrast between the smooth topology 230 and rough topology 220. Specifically, it is especially important to fabricate a rough topology which has less reflectivity than the smooth topology. This poses a significant problem when using planar process technologies.

As described in the Background section, a planarized process emphasizes planar topologies. This leads to poor reflective contrast between different materials and structures. For example, Fig. 3 shows a contact 305 formed using a planarized process with plug technology. Contact opening 305 is formed through oxide 310 to substrate 320. Substrate 320 is typically silicon, but may be another material such as germanium or gallium arsenide.

Contact opening 305 is filled with a plug 330, which is a conductive material. Plug 330 is typically tungsten. Plug 330 may be formed using other materials and alloys such as titanium and titanium-tungsten. Effectively, plug layer 330 couples a layer, above and electrically contacting plug 330, to a layer below and electrically contacting plug 330. For example, in Fig. 3, plug layer 330 electrically couples a first metal layer 340 to substrate 320. This type of connection may be used to, for example, ground the substrate.

Plug layer 330 helps produce a flatter topology. Compared to a process without a plug layer, a step 350 between plug 330 and oxide 310 is minimized. Therefore, the resulting topology is smoother and flatter. As a result, subsequent layers stacked over plug layer 330, oxide 310, and step 350 will also be smoother and more planar. In some processes, the topology may even be planarized further by chemical-mechanical polishing (CMP), where the surface of oxide layer 310 is polished (or ground) to ensure its flatness. Therefore, using a planar process, it becomes increasingly difficult to create a rough regions on layer 340 which may be used as an alignment target.

Plug technology may be used similarly for vias between two metal layers. A plug material would fill the via and minimize a step between the oxide and via opening. This helps produce a planar topology in a similar way for vias as described above for contact openings.

Fig. 4 shows a cross-sectional view of alignment target 230 along the line 250 to 255 of Fig. 2A. A region with rough topology 410 has on either side, regions with smooth topology 415. This rough topology structure may be formed using a planarized process.

In the present invention, to form a rough topology region 410, a field oxide layer 420 is formed on a substrate 425. By forming the structure on field oxide, this helps ensure that the substrate is not accidentally shorted. A polysilicon layer 430 is formed on field oxide layer 420. A contact opening 433 having a lateral dimension exceeding a minimum contact size is formed in an oxide layer above polysilicon 430 to create a contact layer 435. As shown, there may be multiple contact openings 433 in contact layer 435 depending on the size of the structure desired.

The process technology defines a minimum contact size. In a planarized process, non-minimum-sized contacts are not typically permitted since the process has been optimized for minimum-sized contacts. Further, using minimum-sized contacts reduces die size. The minimum contact size may be embodied in a design rule for the layout. For example, a minimum contact size may be about one micron. In order to minimize contact resistance, a number of minimum-sized contacts may be used to contact two different materials. Furthermore, this minimum contact size applies to the lateral dimensions; so, a minimum-sized contact typically is a square structure.

In contrast, in rough topology region 410, at least one lateral dimension of the contact opening exceeds a minimum contact size. Therefore, a shape of the contact opening may be rectangular (or other shape), and not necessarily square. For example, if the minimum contact size is one micron, contact opening 433 may have one lateral dimension of 1.5

microns. In a specific embodiment of the present invention, the nonminimum lateral dimension of contact opening 433 should be at least about 1.5 times larger than the minimum contact size. For example, for a 1.0 micron minimum, contact opening 433 should have a lateral dimension of about 1.5 microns or greater. Generally, the larger the contact opening, the bigger the depression in the cored region.

Figs. 5, 6, 7, and 8 show the process steps in more detail. Fig. 5 shows contact opening 433. Fig. 6 shows how contact opening is filled with a first plug layer 610. First plug layer 610 is deposited over the entire surface of the wafer. First plug layer 610 is "etched back" to the contact opening. The etch back process results in a removal of the first plug layer as indicated by dashed line 620. After etch back, for a minimum-sized contact opening, the result is the substantially planarized plug surface as shown in Fig. 3. The surface may be planarized further using chemical-mechanical polishing.

In contrast, for a larger than minimum contact opening, the result is shown in Fig. 7. More specifically, the etch back step creates a nonplanar, cored region 710 in the plug at about the middle of the contact opening. The cored region has a first depression 720. In some cases, etch back may also result in the first depression extending into a process layer 730 beneath the contact. For example, referring to the structure shown in Fig. 4, the first depression could extend into polysilicon layer 430. Because it is nonplanar, the cored region will scatter incident light. By forming a plurality of cored regions (such as shown in Fig. 4) in a plurality of contact openings, a rough topology region may be formed on the wafer.

Fig. 8 shows the plug created by the process sequence shown in Fig. 7 after deposition of a top metal 840. Due to cored region 720 of plug 610, metal step coverage is poor in a region 810. Compared to a relatively flat portion 850 of metal 840, region 810 forms a rough topology region. Metal (especially when processed without antireflective coatings) provides a very good reflective property on smooth

topology 850, but scatters incident light over rough topology 810.

As discussed above, to form a cored region, a contact opening should be larger than minimum size. In a specific embodiment, a lateral dimension of the contact opening should be approximately 1.5 times or larger than the minimum size. For example, if the minimum contact size is 1.0 micron, to form a cored region, the contact opening should be about 1.5 microns or greater.

Returning to Fig. 4, contact opening 433 has a plug layer which has a cored region having a depression, similar to that described for Fig. 7. By stacking subsequent process layers on top of this cored plug region, this aggravates the coring and depression, and the roughness is magnified.

In Fig. 4, a metal-1 layer 440 is formed above contact layer 435 and contact 433. The resulting metal-1 layer 440 is nonplanar over cored region of contact 433, and has a second depression 443. This further enhances the roughness of the topology.

Vias may also be formed using a planarized plug technology, similar to that described for contacts. Specifically, an oxide layer is formed above metal-1 layer 440 to create a via-1 layer 448. A plug layer in a via-1 opening 451 is etched back and cored. As in the case of a contact opening, to facilitate the coring, this via opening is greater than minimum size. And in a specific embodiment of the present invention, the via opening should be about 1.5 times or greater a minimum via size. The coring of via-1 layer 448 is exaggerated because the via opening is formed top of the depression in metal-1 and cored region of contact 433. This further enhances roughness.

A metal-2 layer 453 is formed on top of via-1 layer 448. Similar to metal-1 layer 440, metal-2 layer 453 will be nonplanar and have a depression in the cored region. In fact, at this point in the processing, due to the severe depressions caused by stacking layers over the cored regions, step coverage over the depressed regions may be so severe that

metal-2 does not entirely cover the plug layer in via-1 opening 451.

Further process layers are similarly formed above the cored regions, and will aggravate the coring further, leading to even greater roughness in the topology. For a three-layer metal process, a via-2 layer 455 is formed above metal-2 layer 453. The plug layer in a via-2 opening 458 is etched back and cored. A metal-3 layer 461 is subsequently formed over via-2 layer 455. As shown in Fig. 4, the step coverage may be extremely severe so metal-3 layer becomes discontinuous and not cover the plug layer in via-2 opening 458. Note that a void 465 may be formed above the cored regions due to severe step coverage caused by the cored regions.

In other embodiments of this invention it may not be necessary to have multiple stacking layers to provide the final surface for light reflection contrast. For example, in a three-layer metal process, a stack formed using (metal-3)-(via-2)-(metal-2) may be sufficient to create enough surface roughness for contrast. In another example of five-layer metal process, a stack formed using (metal-5)-(via-4)-(metal-4)-(via-3)-(metal-3) may be required to provide the necessary surface roughness.

The structure and typically the entire wafer is covered with a passivation or insulating layer 468. Layer 468 may be a single layer material such as oxynitride, or multiple layers of material such as oxide, nitride, and polyimide. Passivation layer 468 may have cracks (not shown) over the cored regions 465. Passivation layer 468 over the alignment structure may be removed to enhance the difference in the reflectivity between the smooth and rough regions. In a specific embodiment, the passivation is removed from over rough region. This process also removes an antireflective coating 463 from the metal enhancing reflectivity from smooth topology regions.

The topologically rough region formed, as described above, will scatter incident radiation, in contrast to a topologically smooth region, which reflects light. This

difference in reflectivity, or reflectivity contrast, may be used by an alignment system for aligning integrated circuits and wafers.

The foregoing description of preferred embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form described, and many modifications and variations are possible in light of the teaching above.

For example, although described for a three-layer metal process, the technique and structure of the present invention will be equally applicable to a single-metal and double-metal process. In those cases, the contact layer is cored, and subsequent via layers, if any, are also cored. This would result in structure with a rough topology useful for an alignment structure.

Furthermore, varying degrees of contrast in reflectivity may be achieved by selecting or limiting the number of layers which are cored. For example, in a three-layer metal process, only the via-1 layer may be cored to create a region with a first degree of reflectivity. In another region, the contact and via-1 layers may be cored to create a second degree of reflectivity. An alignment system may use these varying degrees of reflectivity for more precise alignment of the integrated circuit.

A process may also have additional layers such as added metal and via layers. This additional layers may be cored and stacked on the already cored, nonplanar regions to further enhance the rough topology.

The embodiments were chosen and described in order to best explain the principles of the invention and its practical applications to thereby enable others skilled in the art to best utilize the invention in various embodiments and with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the claims appended hereto.